REMARKS

Claims 1-34 and 36 are now pending in this application. By this response to the non-final Office Action dated July 5, 2006, claims 1-18, 20, 25, and 26 are amended, and claims 35 and 37 are canceled. Care has been taken to avoid the introduction of new matter. Favorable reconsideration of the application in light of the following comments is respectfully solicited.

Rejections Under 35 U.S.C. § 112 ¶ 2

On page 3 of the Office Action, claims 1-37 are rejected under 35 U.S.C. § 112 ¶ 2 as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In response, Applicants have amended claims 1-18, 20, 25, and 26, and respectfully request reconsideration of the rejections.

Specifically with respect to claims 1 and 2, Applicants have amended the claims to address the cited bases of rejection by way of further clarification.

Specifically with respect to claims 3-5, 7, and 9-12, the Office Action states that "the term 'current frequency component' is unclear." In response, claims 3-12 have been amended to recite "a current component at each frequency," which is supported, for example, by Fig. 9, numeral 902.

Specifically with respect to claims 5, 10, and 11, the Office Action states that "the term 'a predetermined threshold' is unclear." In response, the claims have been amended to recite "a predetermined threshold *number*."

Specifically with respect to claim 21, one exemplary embodiment by which a resistance and capacitance can be used to calculate the equivalent resistance and capacitance of the entire chip is depicted, for example, in Fig. 72. An equivalent resistance can be made by averaging all resistance between nodes of a netlist. An equivalent capacitance can be made by summing all

capacitance between the power supply line and the target signal line. "[C]alculating the correction coefficient by performing processing according to a table prepared in advance" can be, for example, the table representing the relationship between a correction coefficient and an equivalent resistance and an equivalent capacitance.

Specifically with respect to claim 22, one exemplary embodiment by which a resistance and capacitance can be used to calculate the equivalent resistance and capacitance of the entire chip is depicted, for example, in Fig. 64. One exemplary embodiment, as depicted in numerals 8101 and 8102, can store resistance and capacitance information of the entire chip extracted by the LPE tool from layout information. One exemplary embodiment for "calculating the correction coefficient by performing processing according to a mathematical expression prepared in advance" is depicted, for example, in Fig. 69, numeral 8607 (*see, e.g.*, pp. 159-60 (paragraphs labeled [0304] and [0305]).

Specifically with respect to claim 23, an example of the recited "base of the event-based model" is depicted as Fig. 67, label "T" (*see, e.g.*, pp. 116-17 (paragraphs [0225]-[0228]).

Specifically with respect to claim 24, an example of the recited "area of the event-based model" is depicted as Fig. 67, label "I" (*see, e.g.*, pp. 116-17 (paragraphs [0225]-[0228]). The amount of a current can be estimated as the area of an event-based model.

Specifically with respect to claim 25, the amount of current can be estimated, for example, as the shape information of an event-based model of a current waveform. As depicted in the example of Fig. 67, such shape information can include a base length and an area, and can be used to calculate the equivalent information of the chip by, for example, estimating a base length and an area of the event-based model.

Specifically with respect to claim 27, the number of transistors included in the chip can be estimated, for example, by considering an area of the chip. From this, the equivalent resistance and equivalent capacitance can be estimated. This method of analysis can be employed at the specification generation stage, when the area of the chip can be estimated.

Specifically with respect to claim 28, in one exemplary embodiment, the technology information may include the dielectric constant between wire layers determined at the specification generation stage, the resistance value of the power supply wire sheet determined at the specification generation stage, and other applicable technology determined at the specification generation stage (*see* pp. 136-37, paragraph [0264]).

Specifically with respect to claim 29, one exemplary embodiment makes it is possible to estimate the equivalent resistance and equivalent capacitance by considering the chip shape, as the chip shape and area information can yield the deflection of the layout of pads and wirings. Furthermore, the power supply pad position can have an effect on equivalent resistance and equivalent capacitance.

Specifically with respect to claim 30, the area of the chip and the number of power supply pads can provide information about the distance between pads, which can affect the estimated equivalent resistance and equivalent capacitance.

Specifically with respect to claim 31, the width of the power supply wire can provide information about the estimated equivalent resistance and equivalent capacitance.

Specifically with respect to claim 32, decoupling capacitance cells can be laid out in a specified area under the power supply wires to reduce the fluctuation of the voltage level of the power supply wires. This area of capacitance can provide information for more accurately estimating the equivalent resistance and equivalent capacitance.

Specifically with respect to claims 33 and 34, examples of "module[s]" are macro circuits having some function, such as a standard logic module or RAM, as depicted in Fig. 83. The "correction coefficient" can be for an event-based model of an estimated current waveform.

For the reasons discussed above, Applicants submit that the pending claims are allowable with respect to 35 U.S.C. § 112 ¶ 2, and Applicants respectfully request withdrawal of the rejections.

Rejections Under 35 U.S.C. §§ 101, 112 ¶ 1

On page 12 of the Office Action, the claims are rejected under 35 U.S.C. §§ 101 and 112 ¶ 1. Though traversed, in order to expedite examination of the application, it is submitted that the alleged issues raised have been obviated by the enclosed amendments (which are submitted without prejudice/disclaimer to the subject matter embodied thereby). Applicants submit that the pending claims are allowable with respect to 35 U.S.C. §§ 101 and 112, and respectfully request withdrawal of the rejections.

Rejection Under 35 U.S.C. § 103(a)

In section 5 of the Office Action, claims 1-3, 20, and 26 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Hayashi et al., "EMI-Noise Analysis under ASIC Design Environment," ACM Press, 1999, pages 16-21 ("Hayashi"). Claims 1, 20, and 26 are independent. Applicants respectfully traverse.

With respect to claim 1, Hayashi does not teach or suggest "a method of analyzing . . . including . . . allocating a *discrete* FFT analysis frequency width in *each* frequency range," as recited in claim 1. The Office Action acknowledges that "Hayashi does not explicitly disclose performing the FFTs by first breaking the signal into frequency bins." The Office Action alleges that the allocation of frequency widths as claimed is nevertheless obvious because "[t]he skilled

artisan would also know that the widths of the FFTs can be altered through the use of any well-known windowing function." This allegation lacks factual support that such a modification was within the skill of an artisan or simply known within the art at the time of invention, and there is no support, explicitly or implicitly, in Hayashi for such an allegation. Applicants' specification discusses prior art implementations which made use of a width of a predetermined single value, contrasting them with the claimed use of frequency widths, which allows for an "FFT result [which] can be obtained at a higher speed and with a smaller memory while maintaining the precision." (*see, e.g.*, pp. 12-13 (labeled ¶ [0029]); *compare* Fig. 5 (an illustration of the "conventional method") with Fig. 10 (exemplary frequency widths)).

The Office Action merely discounts the claimed features admittedly not disclosed by Hayashi as allegedly being obvious without support whatsoever from the cited prior art. Applicants respectfully point to MPEP § 2143.03 under the section entitled "All Claim Limitations Must Be Taught or Suggested", which sets forth the applicable standard for establishing obviousness under § 103:

> To establish *prima facie* obviousness of a claimed invention, ***all*** the claim limitations must be taught or suggested ***by the prior art.*** (citing *In re Royka*, 180 USPQ 580 (CCPA 1974)).

In the instant case, the pending rejection does not "establish *prima facie* obviousness of [the] claimed invention" as recited in claim 1 because the cited prior art does not fulfill "all the claim limitations" standard required under § 103. The Office Action fails to identify any portions of the cited prior art which allegedly suggest the claimed structure. What the *Examiner* believes to be obvious is irrelevant in determining patentability under § 103.

In this regard, it is respectfully submitted that the Office Action has merely concluded that the claimed invention would have been obvious based on the Examiner's own ***opinion***,

which is not commensurate with the requirements under § 103. Accordingly, absent any prior art teachings of the specific features recited in the claims, the pending rejection is based solely on improper hindsight reasoning using only Applicants' specification as a guide to reconstruct the claimed invention. The "Examiner's opinion" can not be relied on to replace the deficiency of a prior art reference.

If the Examiner intended to take Official Notice that the differences between the present invention and cited prior art and/or the motivation to modify Hayashi are well-known in the art, then pursuant to MPEP § 2144.03, Applicants respectfully traverse such an assertion and **request the Examiner to cite a reference in support of his position** (*see* second paragraph, last three lines of MPEP § 2144.03, requiring the Examiner to cite a reference in support of his allegation of Official Notice when Applicants traverse). Indeed, only Applicants' specification discloses the claimed features, and supplies the motivation for providing them within the particular combination recited in claim 1.

At best, the basis for the rejection amounts to nothing more than a general allegation that one of ordinary skill in the art ***can*** achieve the claimed invention, which is not a proper standard by which to make a rejection under § 103. MPEP § 2143.03 under the subsection entitled "Fact that References Can Be Combined or Modified is Not Sufficient to Establish *Prima Facie* Obviousness", sets forth the proper standard:

> The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. (*In re Mills*, 16 USPQ2d 1430 (Fed. Cir. 1990)).

In the instant case, even assuming *arguendo* that Hayashi can be modified to reach the claimed invention, it is submitted that the "mere fact that [the reference] can be . . . modified . . . does not render the resultant modification obvious" because nowhere does the ***prior art*** "suggest

the desirability of the [modification]" as set forth by the Examiner. Without the necessary factual support for the allegation that the prior art includes knowledge of the use of frequency widths as claimed, no *prima facie* case of obviousness can be sustained against claims 1-3.

Claim 20 recites "calculating a correction coefficient; and . . . correcting, by using the correction coefficient." Claim 26 similarly recites "calculating a correction coefficient." Applicants respectfully point out that the Office Action does not address these limitations. In imposing a rejection under 35 U.S.C. §103, the Examiner is required to point to "page and line" wherein an applied reference is perceived to identically disclose each feature of a claimed invention. *In re Rijckaert*, 9 F.3d 1531, 28 USPQ2d 1955 (Fed. Cir. 1993); *Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 221 USPQ 481 (Fed. Cir. 1984). Moreover, it is respectfully submitted that Hayashi does not teach or suggest such a coefficient, nor is there disclosed motivation for an artisan to modify the teachings of Hayashi to calculate or make use of such a coefficient in the manner referenced in the corresponding claims. Therefore, claim 20 is patentable over Hayashi.

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as claims 1, 20 and 26 are patentable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also patentable. In addition, it is respectfully submitted that the dependent claims are patentable based on their own merits by adding novel and non-obvious features to the combination.

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Based on the foregoing, it is respectfully submitted that all pending claims are patentable over the cited prior art. Accordingly, it is respectfully requested that the rejections under 35 U.S.C. § 103 be withdrawn.

For the above reasons, Applicants submit that the application is in condition for allowance, and respectfully request its reconsideration.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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